Benchmarking Semiconductor Manufacturing

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Background

• Under the leadership of Ralph Gomory, the Alfred Sloan Foundation funded a number of *industry centers* at leading US universities

• U C Berkeley was invited to develop a semiconductor industry center

• We called our center the *Competitive Semiconductor Manufacturing* (CSM) Program and we focused on fabrication of microelectronics

• Initial funding from Sloan Foundation 1991 – 1995, then industry funding 1996 – 2003
CSM Program

• What we did 1991 - 2003:
  • Developed practical metrics of manufacturing performance
  • Studied performance and practices at 100 fabs worldwide
  • Identified best practices underlying top metric scores
  • Conducted focus studies (MS and PhD projects within traditional disciplines)
Industry starting point - 1991

• Planar fabrication process was standard across industry
• Standard equipment ("process tools") and materials available across industry
• Japanese manufacturers achieved superior yields and had made large capital investments
What are the challenges of semi manuf?

• New process technology and product generation (shrink) every 2-3 years
• Initially, a new process does not work – poor yield, long cycle time, poor equipment productivity
• Products of a given process technology go obsolete fast, prices decline exponentially with time
• It’s a race to de-bug process, ramp volume and reduce cycle time before prices drop
• Must quote and meet delivery dates (customers run their own factories)
Samsung’s average DRAM selling prices
What was done to fix quality and yield?

• Berkeley and Stanford developed design software (“EDA” or “electronic design automation”)
  • Incorporates design rules reflecting factory capabilities
  • Less incompatibilities between design and manufacturing

• Ultimately led to disaggregation of industry into “fabless” design - marketing companies and “foundry” contract manufacturers
What was done to fix quality and yield?

• Manage the distributed development of unit processes
  • *FMEA* (failure modes and effects analysis) – identify all failure modes of a unit process, design tests integrated into the unit process to prove failure modes do not exist before passing WIP (work-in-process) to next unit process
  • *Design for testability* – design-in features to product or to unit process to make it easier to test or easier to measure

• Routinely amass complete audit trail of exactly what happened
  • Process data, metrology data, equipment data, WIP data, test data, all integrated
  • No keystrokes – connect all equipment to host
What was done to fix quality and yield?

• Conduct thorough statistical analysis of yield losses ...
Figure 2. Example Yield Histogram

No. of wafers

Baseline defect-limited yield

Impact of systematic mechanisms

Yield (%)
What was done to fix quality and yield?

- **Top-down analysis**: Deduce baseline defect-limited yield and systematic mechanisms-limited yield
  - *Baseline defect loss* – no signature, equally likely anywhere and anytime
  - *Systematic loss* – has spatial or temporal signature (process failed, bursts of particle contamination, etc.)

- **Bottom-up analysis**: Conduct thorough failure analysis to identify root causes and track frequencies and scope of various types of yield losses

- Compare *bottom-up* and *top-down* analyses of yield losses to track progress and infer how much loss remains to be explained
Example bottom-up analysis

Yield loss (total 21%)

- Identified systematic losses
  - Parametric test 3.1%
  - Missing metal islands (scanner leveling issue) 2.9%
  - Missing implant layer islands 1.2%
  - Wafer edge losses (voids, peeling) 5.8%
  - Defect excursion losses (Specific source tools identified) 7%

- Baseline defects (total 23%)
  - STI HDP particles 0.3%
  - Contact pattern fail 3.8%
  - M1 – M5 pattern fails 3.8%
  - Poly 1 pattern fail 1.5%
  - Poly 1 particles 0.5%
  - etc
Best practice: tracking bottom-up vs. top-down

- Actual yield
- Target yield
- Actual yield + planned fixes of identified losses
- Identification needed, solutions needed
What was done to fix quality and yield?

• For important process parameters, perform automated statistical process control (SPC)
  • Stop process and/or equipment when unlikely statistics arise
  • Automatically notify responsible engineer and investigate

• Practice advanced process control
  • FDC (fault and defect classification)
  • Feedback control
  • Feedforward control

• Increase in-line metrology and in-line testing
  • Find problems as early as possible

• Practice six-sigma analysis
  • Prioritize process problems
What was done to reduce cycle time?

• Make wise equipment investments
  • Determining the bare-minimum equipment set is straightforward, but it results in an exorbitant cycle time
  • What extra equipment to buy?
  • Analysis to determine cycle time reduction for an additional tool for each tool type
  • Add equipment to the bare-minimum set in order of most cycle time reduction per capital dollar
Cycle time-optimized capex

- Baseline tool set (0% surge, CT = 203 days)
- Judgmental plan (CT = 120)
- Same CT for $491M less capex
- Half the CT for $192M less capex
What was done to reduce cycle time?

• Improve factory execution
  • Introduce advanced planning and dispatching whereby dispatching decisions are based on factory-wide analysis
    • Maintain good WIP profile through process
    • Maintain bottleneck utilization
  • Change scheduling paradigm from lot-based dispatching (which lot) to volume-based dispatching (how much of each product-step)
  • Where dispatching cannot balance utilization, introduce advanced scheduling
Target WIP profile

- Ideal Production Quantity = (Target output due over the target cycle time to fab out plus one shift) - (actual downstream WIP)
What Happened in the Semi Industry

• Early 1990s: Considerable closure in yield performance
• Late 1990s: Disparity in speed and on-time-delivery performance
  • Mostly reflecting sophistication of execution
• Late 1990s: Disparity in productivity performance
  • Mostly reflecting economies of scale ("small fabs are bad fabs")
  • Helped drive fabless-foundry split
• CSM program showed that by 2000, speed differences were economically about twice as significant as cost differences
What Happened in the Semi Industry

• In 1988, Japanese companies had ~ 51% of global semiconductor sales
• In 2005, Japanese companies had ~ 22% of global semiconductor sales
• In 1988, US companies had ~ 37% of global semiconductor sales
• In 2005, US companies had ~ 49% of global semiconductor sales
• In 1980s, the big swallowed the small
• In the 1990s, the fast ran over the slow
What Happened in the Semi Industry

- Cycle time per mask layer dropped from ~2.5 days to ~1.0 day
- Mature yield for CPU chips rose from ~82% to ~92%
- Photo tool productivity rose from ~400 wafers per tool per day to ~1000 wafers per tool per day
- Time to ramp to mature yield dropped from ~24 months to ~12 months
- The “Berkeley metrics” were adopted by all major industry associations and most individual companies
  - Fab performance no longer had any geographical signature
Thank you for your attention!

• You are welcome to email me any questions or comments: leachman@Berkeley.edu

• And if you would like a copy of a semiconductor benchmarking report or this presentation, just email me a request.